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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): 41160/RRT/B600

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on September 7, 2005

Signature: Christina L. Vann

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Application Number	Filed
09/651,425	8/30/2000

First Named Inventor: Christopher Songer

Art Unit	Examiner
2193	Tuan A. Vu

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [XX] attorney or agent of record. Registration number 43,945
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

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September 7, 2005
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

- [ ] *Total of _____ forms are submitted.

REMARKS FOR PRE-APPEAL BRIEF REQUEST FOR REVIEW

Claims 1-44 are pending in this application. Claims 1-17, 19-38, and 41-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over 1) Tseng et al. (U.S. 6,009,256), in view of 2) Schlansker et al. (U.S. 6,408,428), and in further view of 3) Trimberger (U.S. 5,752,035).

To establish a *prima facie* case of obviousness, the Examiner must establish that the cited references, combined, teach or suggest each of the elements of a claim. In regard to claim 1, this claim include the elements of "partitioning the processing element array into a plurality of hardware accelerators; identifying a plurality of functions in a program source code that are anticipated to consume a substantial execution time; decomposing the program source code into a plurality of kernel sections, wherein the identified plurality of functions are recognized as the plurality of kernel sections; mapping said plurality of kernel sections into a plurality of hardware dependent executable code for execution on the plurality of hardware accelerators; and forming a matrix describing different combinations of said plurality of hardware accelerators, code variants and said hardware dependent executable code to support run time execution of the plurality of kernel sections by the processing element array, wherein each code variant performs a function whose inputs and outputs are identical." Appellant believes that the Patent Office has failed to establish that the cited references teach or suggest each of these elements of claim 1 and therefore has failed to establish a *prima facie* case of obviousness for claim 1.

In regard to the element of "partitioning the processing element array into a plurality of hardware accelerators," the Examiner has relied on Tseng et al. to teach this element. However, the system of Tseng dose not partition "the processing element array into a plurality of hardware accelerators." Rather, the system of Tseng maps and partitions those portions of the circuit design that have been modeled in hardware into the FPGA chips in the reconfigurable hardware boards 250. (Col. 16, lines 47-50). That is, the reconfigurable hardware boards of Tseng are not the equivalents of the processing element array of the present invention that are capable of executing the code

Regarding the element of "identifying a plurality of functions in a program source code that are anticipated to consume a substantial execution time," the Examiner relies on the language "the most frequently executed code and replac[ing] it with programmable instructions

unit, or accelerator set (e.g. col. 6, lines 31-56)," in Trimberger to teach this element. However, a "most frequently executed code" is not the same as code "that are anticipated to consume a substantial execution time." For example, a small piece of code that takes very little time to execute may be a "most frequently executed code" that does NOT consume a substantial execution time. Furthermore, a general optimization process (or the reason for optimization) does not necessarily teach "identifying a plurality of functions in a program source code that are anticipated to consume a substantial execution time." (See, Final Office action dated June 12, 2005, middle of page 14). In fact, by only generating hardware models for the combinational and register components that are relatively simple components (see, e.g., col. 17, lines 35-42, cited above), the system of Tseng teaches away from "identifying a plurality of functions in a program source code that are anticipated to consume a substantial execution time."

Regarding element "mapping said plurality of kernel sections [that are anticipated to consume a substantial execution time] into a plurality of hardware dependent executable code for execution on the plurality of hardware accelerators," the Examiner admits that Tseng "does not explicitly disclose the mapping in (i) is a matrix mapping of kernel sections into a plurality of hardware dependent executable code." (Final Office action (6/15/05), page 3, last paragraph.). However, the Examiner states that this "mapping is suggested by "RTL level signal used in program to effect signaling of a FPGA and support emulation/simulation/debug of hardware. (Id., page 4). However, this alleged "RTL mapping" is not the same as "mapping said plurality of kernel sections into a plurality of hardware dependent executable code for execution on the plurality of hardware accelerators."

Regarding element "forming a matrix describing different combinations of said plurality of hardware accelerators, code variants and said hardware dependent executable code to support run time execution of the plurality of kernel sections by the processing element array, wherein each code variant performs a function whose inputs and outputs are identical," the Examiner again relies on Tseng et al. to teach this element.

First, the system of Tseng "maps the selected hardware models into a reconfigurable hardware emulation board. In particular, step 307 takes "the netlist and maps the circuit design into specific FPGA chips." (Tseng et al., col. 19, lines 14-20). Tseng et al further teaches that "step 309 generates the configuration files for mapping the hardware model to FPGA chips. In essence, step 309 assigns circuit design components to specific cells or gate level components in

each chip." (Tseng et al., col. 19, lines 55-61). Accordingly, there is no teaching or suggestion in Tseng of "a matrix describing different combinations of said plurality of hardware accelerators, said hardware dependent executable code, and variants."

Second, the system of Tseng does not generate code "to support run time execution of the plurality of kernel sections by the processing element array." Rather, the executable code of Tseng is run by the processor/workstation 240, not by the FPGA chips.

As a result, the Patent Office has failed to establish that the cited references teach or suggest each of these elements of claim 1 and therefore has failed to establish a *prima facie* case of obviousness for claim 1.

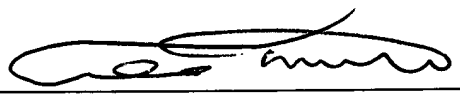
Additionally, the alleged combination of the three references, Tseng, Kolchinsky, and Trimberger and an alleged equivalency requires a series of separate, awkward combinative steps that are too involved to be considered obvious. The fact that three different references are combined with an equivalent step (total of four steps), indicates that claim 1 is not obvious in view of cited references.

Claims 18, 39, and 40 include similar elements as the elements of claim 1, therefore, a *prima facie* case of obviousness for these claims is also not established.

Accordingly, it is submitted that the rejections of claims 1 18, 39, and 40, and their respective dependent claims based on 35 U.S.C. § 103 be overturned.

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By 

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